IN THE CLAIMS

Claim 1. (Currently amended) A memory device structure, comprising:

a substrate;

a gate oxide layer disposed on a portion of the substrate;

a gate disposed on the gate oxide layer, wherein the gate and the gate oxide layer form a gate structure;

a buried bit line disposed in the substrate along both sides of the gate;

a raised line disposed on the buried bit line;

a spacer disposed on both sidewalls of the gate structure, thus electrically isolating the gate and the raised line, wherein a top of the raised line is lower than a top of the spacer;

a word line disposed on the gate in a direction perpendicular to the buried bit line; and

an insulation layer disposed on thea top of the raised line to electrically isolate the word line and the raised line.

Claim 2. (Original) The structure as claimed in claim 1, wherein a material for forming the insulation layer comprises silicon oxide.

Claim 3. (Original) The structure as claimed in claim 1, wherein a material for forming the spacer comprises silicon oxide.

Claim 4. (Original) The structure as claimed in claim 1, wherein a material for forming the raised line comprises polysilicon.

Claim 5. (Original) The structure as claimed in claim 1, wherein a material for forming the word line comprises polysilicon.

Claim 6. (Original) The structure as claimed in claim 1, wherein the buried bit line is a shallow junction buried bit line.

Claims 7-18. Previously withdrawn.